Withdrawal of the rejection of claims 1-4, 9-10, 13-18, 21-30, and 32 under 35 U.S.C. §102(b) as being anticipated by Kaneko et al. (US 5,534,786) is requested.

Applicants note that anticipation requires the disclosure, in a prior art reference, of each and every limitation as set forth in the claims.[1] There must be no difference between the claimed invention and reference disclosure for an anticipation rejection under 35 U.S.C. §102.[2] To properly anticipate a claim, the reference must teach every element of the claim.[3] "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference".[4] "The identical invention must be shown in as complete detail as is contained in the ...claim."[5] In determining anticipation, no claim limitation may be ignored.[6] At least with respect to independent claims 1, 30, and 32, the applied art does not meet the requirements for anticipation set forth above, as discussed below.

By way of background, the present application, in a preferred embodiment, is directed to a carrier for test, burn-in, and first-level packaging of semiconductor devices. The disclosed and claimed invention provides, in one aspect of the invention, a method for manufacturing and testing semiconductor components that combines testing, burning-in and end-use packaging. In another aspect of the invention, a semiconductor structure comprising a device carrier is provided, wherein the carrier used for burn-in testing is also used in the end-use application, without removing the device from the carrier.

The components or semiconductor devices attached to the carrier are tested via interconnect wiring in the carrier. The wiring in the carrier is also sufficient for end-use operation of attached semiconductor devices. The carrier is divided into a plurality of components such that each component contains at least one semiconductor device, for example. Those components, including the carrier, are used as the first packaging level of assembly.

---

[1] *Titanium Metals Corp. v. Banner*, 227 USPQ 773 (Fed. Cir. 1985).
[2] *Scripps Clinic and Research Foundation v. Genentech, Inc.*, 18 USPQ2d 1001 (Fed. Cir. 1991).
[3] *See* MPEP § 2131.
[4] *Verdegaal Bros. v. Union Oil Co. of Calif.*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).
[5] *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).
[6] *Pac-Tex, Inc. v. Amerace Corp.*, 14 USPQ2d 187 (Fed. Cir. 1990).

By the method and structure of the claimed invention, the substantial costs and time associated with initially aligning and attaching chips to the substrate to conduct burn-in, and then removing the chips, separately testing the chip characteristics in a tester, and then reattaching the chips to a final substrate once burn-in and device characterization are completed are avoided by using the burn-in test carrier as part of the end-use package.

In contrast, Kaneko et al. is discloses a burn-in and test method of semiconductor wafers and burn-in boards for use in semiconductor burn-in tests which divides each semiconductor wafer into blocks each including some integrated circuits, and which assigns each block an address to indicate in which part of the semiconductor wafer the integrated circuits of the block are placed. These addresses are recorded, and detachable carriers also having an identification code are loaded with a block to be tested. As discussed in Kaneko et al. (see col. 5, lines 7-13 when all the burn-in is finished, all carriers are removed from the burn-in board, and then, these carriers are fitted in the IC sockets of an IC tester for testing their characteristics. By handling and loading plural dies in block units, electrical connections to the burn-in and test apparatus are not as complicated, and the procedure is not a laborious as with so-called "die-by-die" loading.

Analysis of burn-in test results permits the locating of defective integrated circuits in semiconductor wafers using the recorded addresses of the blocks, and the identification codes of the carriers. Once "good" chips are identified, they are removed from the carrier, and subsequently reattached to an operational carrier.

Kaneko et al., therefore, represents a conventional, expensive and time-consuming temporary chip attachment, which is specifically disfavored by the approach in the present application. Contrary to the assertion in the Official Action, Kaneko et al. does not disclose a device carrier used for both burn-in testing and end use operation of the semiconductor devices contained therein.

In particular, Kaneko et al. does not disclose a method for manufacturing and testing semiconductor components which includes, among other features, "...providing a device

carrier...having interconnect wiring...sufficient for both testing and end use operation of said semiconductor device", as recited in independent claim 1.

Further, Kaneko et al. does not disclose a semiconductor structure which includes, among other features, "a device carrier...having interconnect wiring...sufficient for both testing and end use operation of said semiconductor devices...without separating said devices form said carrier", as recited in independent claim 30.

Finally, Kaneko et al. does not disclose, as depicted in one embodiment shown in Figs. 13a and 13b, a semiconductor structure which includes, among other features, "a stack of flex device carriers...and an interconnect substrate, wherein said flex device carriers are electrically connected to said interconnect substrate", as recited in independent claim 32.

Accordingly, since the applied art does not disclose all the features of the recited invention, withdrawal of the anticipation rejection and allowance of independent claims 1, 30, and 32 are requested.

Further, as dependent claims 2-29, depending from independent claim 1, and dependent claim 31, depending from independent claim 30 incorporate the allowable subject matter of the respective independent claims, these claims are submitted as being allowable at least on that basis, as well as in their own right. Allowance of dependent claims 2-29 and 31 are requested.

For example, dependent claim 2 recites the additional step of "installing one said component on a next level of assembly without separating said device from said carrier."

Kaneko et al. clearly discloses the opposite of this dependent claim recitation, by teaching that, after "good" chips are identified, they are removed from the carrier used in the burn-in test, and subsequently fitted into the IC sockets of an IC characteristics tester. Applicant presumes that subsequent removal from the IC tester and attachment to an end-use carrier follows a successful test of the IC characteristics.

As a further example, dependent claim 9, depending ultimately from independent claim 1 and from intervening dependent claims 5, 6, and 7, recites that "said semiconductor devices are organized in a plurality of groups on said carrier wherein BIST pads on said devices in each group are connected in parallel to separate external contacts. Dependent claim 5, from which claim 9 depends, recites the additional step of "...providing a lead reduction mechanism on said carrier...connected to said carrier contacts", while dependent claim 6 recites that the lead reduction engine comprises a built-in-self-test engine.

The Official Action acknowledges the deficiency of Kaneko et al. with respect to disclosing the recitations of dependent claims 5-7, from which claim 9 depends.[7] Therefore, as the applied art does not disclose every feature of Kaneko et al., withdrawal of the anticipation rejection, and allowance of dependent claims 9-10 are requested.

Further, in the event that a Notice of Allowance is not forthcoming in response to this communication, Applicants submit that the next Official Action could only be non-final under proper MPEP procedure, in that either:

(1) The incorrect statutory basis for the anticipation rejection of claims 9-10 under 35 U.S.C. §102 has been set forth, in light of the unpatentability rejection of intervening claims 5-7 over Kaneko et al. in view of Nakata et al. under 35 U.S.C. §103(a) (discussed below); or

(2) The unpatentability rejection of claims 5-7 in the outstanding Official Action was made under the incorrect statutory basis, if the anticipation rejection of claims 9-10 is renewed.

Withdrawal of the rejection of claims 5-8, 11-12, ad19-20, and 31 under 35 U.S.C. §103(a) as being unpatentable over Kaneko et al. in view of Nakata et al. (US 5,945,834) is requested.

[7] *See* Official Action at page 4, paragraph 5.

At the outset, Applicant notes that, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, ***the prior art reference must teach or suggest all the claim limitations*** (emphasis added).[8] Further, the teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure.[9]

Even assuming that the references are properly combinable as suggested by the Examiner, a proposition with which Applicants do not necessarily agree, Nakata et al. does not make up for the previously identified deficiency of Kaneko et al., particularly with respect to providing a teaching or suggestion of a method for manufacturing and testing semiconductor components which includes, among other features, "...providing a device carrier...having interconnect wiring...sufficient for both testing and end use operation of said semiconductor device", as recited in independent claim 1.

Further, Nakata et al. does not make up for the previously identified deficiency of Kaneko et al., particularly with respect to providing a teaching or suggestion of a semiconductor structure which includes, among other features, "a device carrier...having interconnect wiring...sufficient for both testing and end use operation of said semiconductor devices...without separating said devices form said carrier", as recited in independent claim 30.

Since the applied art, taken alone or in combination, does not teach or suggest all the limitations of independent claims 1 and 30, respectively, withdrawal of the rejections, and allowance of dependent claims 5-8, 11-12, ad19-20, and 31 are requested.

---

[8] *See* MPEP §2143.

[9] *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991) and *See* MPEP §2143.

In view of the above, consideration and allowance of claims 1-32 are, therefore, respectfully solicited.

Applicant notes that Formal Drawings have been hand-carried and filed concurrent with the filing of this Response.

In the event the Examiner believes an interview might serve to advance the prosecution of this application in any way, the undersigned attorney is available at the telephone number noted below.

Although extensions of time are not believed to be necessary with this communication, the Director is hereby authorized to charge any fees, or credit any overpayment, associated with this communication, including any extension fees, to CBLH Deposit Account No. 22-0185.

Respectfully submitted,

Larry J. Hume

Larry J. Hume, Reg. No. 44,163
Customer Number 30678
Connolly Bove Lodge & Hutz LLP
1990 M Street, N.W., Suite 800
Washington, D.C. 20036-3425
Telephone: 202-331-7111

LJH/CMF